

ABSTRACT OF THE DISCLOSURE

In accordance with an embodiment of the present invention, a triggering event is initiated to place a processor in a low power state. The voltage from a first voltage regulator supplied to a core of the processor may be lowered to a level at which the processor core becomes non-operational and the processor state is lost. The processor may include a memory region in which the processor state may be stored upon entering the low power state. This memory region may be powered by a second voltage regulator so that its contents are not lost while in the low power state. For one embodiment of the present invention, the processor may additionally include a snoop controller powered by the second voltage regulator. This snoop controller may snoop a cache, which may also be powered by the second voltage regulator, while the processor is in the low power state. The snoop controller may additionally monitor interrupts.